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Applicant: Fernando Gonzalez

Filing Date: August 30, 2001

Group: 2811

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
DLJ	Chang, C., et al., "Enabling Shallow Trench isolation for .01 micrometer Technologies and Beyond", <u>Symposium on VLSI Technology Digest of Technical Papers</u> , pp. 161-162, (1999)
DLJ	Goebel, B., et al., "Vertical N-Channel MOSFETs for Extremely High Density Memories: The Impact of Interface Orientation on Device Performance", <u>IEEE Transactions on Electron Devices</u> , 48(5), pp. 897-906, (May 2001)
DLJ	Matsuda, S., et al., "Novel Corner Rounding Process for Shallow Trench Isolation utilizing MSTs (Micro-Structure Transformation of Silicon)", <u>IEDM</u> , pp. 137-140, (1998)
DLJ	Uh, H., et al., "A Strategy for Long Data Retention Time of 512Mb DRAM with 0.12micrometer Design Rule", <u>Symposium on VLSI Technology Digests of Technical Papers</u> , 2 pages, (2001)

Examiner

Date Considered

3/22/04

*Substitute Disclosure Statement Form (PTO-1449)

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